07-27-04

AF/1700

Attorney's Docket No. 67,200-477

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Chen, et al
Serial No.: 09/ 941,537
Filed: Aug. 29, 2001
For: Method for Reducing Light Reflectance in a Photolithographic Dual Damascene Trench Patterning Process

Group Art Unit: 1756
Examiner: J.S. Ruggles

Commissioner for Patents
Alexandria, VA 22313-1450

TRANSMITTAL OF REVISED APPEAL BRIEF (PATENT APPLICATION-37 CFR 192)

1. Transmitted herewith, in triplicate, is the **REVISED** APPEAL BRIEF in this application, with respect to the Notice of Non-Compliance dated June 25, 2004.

2. STATUS OF APPLICANT
This application is on behalf of:
X other than a small entity.
___ a small entity.

A verified statement:
___ is attached.
___ was already filed.

3. FEE FOR FILING **REVISED** APPEAL BRIEF
Pursuant to 37 CFR 1.17(f), the fee for filing the Appeal Brief is:
____ small entity $165.00
____ other than a small entity $330.00
x was already paid

Appeal Brief fee due: $ 0

Certificate of Mailing

I hereby certify that this correspondence is, on the date shown below, being:

Mailing
X deposited with the U.S. Postal Service with sufficient postage as Express Mail Label No. EV 525 156 546US in an envelope addressed to Mail Stop: Appeal, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Kathy Dixon

Dated: July 21, 2004

4. EXTENSION OF TERM

NOTE: The time periods set forth in 37 CFR 1.192(a) are subject to the provision of □1.136 for patent applications. 37 CFR 1.191(d). See also Notice of November 5, 1985 (1060 O.G. 27).

The proceedings herein are for a patent application and the provisions of 37 CFR 1.136 apply:

(complete (a) or (b), as applicable)

(a) XX Applicant petitions for an extension of time under 37 CFR 1.136 (fees: 37 CFR 1.17(a)-(d) for the total number of months checked below:

	Extension (months)	Fee for other than small entity	Fee for small entity
□	one month	$ 110.00	$ 55.00
□	two months	$ 420.00	$210.00
□	three months	$ 950.00	$475.00
□	four months	$1,480.00	$740.00

Fee: $_____

If an additional extension of time is required, please consider this a petition therefor.

(check and complete the next item, if applicable)

□ An extension for _____ months has already been secured, and the fee paid therefor of $_____ is deducted from the total fee due for the total months of extension now requested.

Extension fee due with this request: $_____

or

(b) □ Applicant believes that no extension of term is required. However, this conditional petition is being made to provide for the possibility that applicant has inadvertently overlooked the need for a petition and fee for extension of time.

5. TOTAL FEE DUE

The total fee due is:

__X__ was already paid
Appeal Brief Fee: $____
Extension fee (if any) $____

TOTAL FEE DUE: $_____

6. FEE PAYMENT

____ Attached is a check in the sum of $ __0__
____ Attached is a Credit Card Payment Form in the amount of $ _0__
A duplicate of this transmittal is attached.

7. FEE DEFICIENCY

NOTE: If there is a fee deficiency and there is no authorization to charge an account, additional fees are necessary to cover the additional time consumed in making up the original deficiency. If the maximum six-month period has expired before the deficiency is noted and corrected, the application is held abandoned. In those instances where authorization to charge is included, processing delays are encountered in returning the papers to the PTO Finance Branch in order to apply these charges prior to action on the cases. Authorization to charge the deposit account for any fee deficiency should be checked. See the Notice of April 7, 1986, 1065 O.G. 31-33.

_X_ If any additional extension and/or fee is required, this is a request therefor and to charge Account No. 50-0484 .

And/Or

_X_ If any additional fee for claims is required, please charge Account No. 50-0484 .

Signature of Attorney

Registration No. 31,311

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U.S.S.N. 09/941,537

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Applicant: Chen et al. Group Art Unit: 1756

Serial No.: 09/941,537 Examiner: J. S. Ruggles

Filed: 08/29/2001

For: METHOD FOR REDUCING LIGHT REFLECTANCE IN A PHOTOLITHOGRAPHIC DUAL DAMASCENE TRENCH PATTERNING PROCESS

Attorney Docket No.: 67,200-477

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 525 156 546 US
Date of Deposit July 21, 2004

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, Alexandria, VA 22313-1450

Kathy Dixon

3d Revised APPEAL BRIEF

Commissioner for Patents
Alexandria, VA 22313-1450

Sir:

APPELLANTS appeal in the captioned application from the Examiner's final rejection, dated 9/11/2003, of claims 1-3, 7-8, 10-11, 13-15, and 17-24 under 35 USC § 103.

It is urged that Examiners final rejection be reversed and that all the claims currently pending be allowed.

(1) REAL PARTY IN INTEREST

The real party in interest in the present appeal is the recorded Assignee, Taiwan Semiconductor Manufacturing Company, Ltd.

(2) RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that are known to the Appellant, the Appellant's legal representative, or the assignee.

(3) STATUS OF CLAIMS

Claims 1-3, 7-8, 10-11, 13-15, and 17-24 are pending in the application.

APPELLANTS have cancelled claims 25 and 26 in the fourth Supplemental Amendment filed together with this Appeal Brief and assume it is entered as suggested by Examiner.

Claims 1-3, 7-8, 10-11, 13-15, and 17-24 stand rejected.

APPELLANTS appeal from the rejection of claims 1-3, 7-8, 10-11, 13-15, and 17-24.

(4) STATUS OF AMENDMENTS

An amendment was filed on or about 07/30/03 which was entered.

A Request for Reconsideration from Final Rejection was mailed 9/11/2003 including proposed amendments was filed on or about 11/10/2003.

An Advisory Action from the Examiner was mailed on 11/28/2003 refusing entry of proposed amendments filed on or about 11/10/2003.

A Notice of Appeal together with a first Supplemental Amendment was filed on or about 12/15/2003 amending the Specification as suggested by Examiner in the Advisory Action and canceling claims 25 and 26 to overcome Examiners objections and rejection of claim 26 under 35 USC Section 112 as well as correcting other defects including grammatical errors.

A second Supplemental Amendment with the Appeal Brief was filed on or about 2/11/ 2004 attempting to insert the language of claim 15 into the Specification to remove an issue on Appeal.

A Notice of Non-compliance with CFR 1.192 was mailed to APPELLANTS on 4/6/2004 together with an Advisory Action alleging errors in APPELLANTS grouping of claims and in the claims as presented in the Appendix primarily related to typographical errors in claim 11 present in the first supplemental amendment and the fact that the Claims Appendix assumed entry of the proposed amendments submitted in APPELLANTS first and second supplemental

amendments. The Advisory action also refused APPELLANTS insertion of the language of claim 15 into the Specification.

A third supplemental amendment was filed on or about 5/06/04 together with a revised Appeal Brief, correcting previously presented grammatical errors in claim 11 present in the proposed first supplemental amendment and amending claim 15 in response to Examiners requirement, as well as attempting to revise the Appeal Brief in accordance with Examiners requirements.

A second advisory action together with a second Notification of Non-Compliance with CFR 1.192 was mailed to APPELLANTS on 6/25/2004 pointing out errors including the now erroneous listing of claims in the Claims Appendix since the third supplemental amendment was not entered due to a failure to double bracket deletions in the Specification and claim 15.

A fourth supplemental amendment has now been filed together with a 3d revised Appeal brief addressing the failure to include double bracketing in proposed amendments made in the Specification and claim 15.

APPELLANTS believe the fourth supplemental amendment complies with all of Examiners objections and assume it will now be entered as indicated by Examiner. APPELLANTS have therefore not appealed from claims 25 and 26 consistent with Examiners guidance in the most recent Notification of Non-Compliance and per Telephone

with Examiner on 7/1/04 and believe the 3d revised Appeal Brief is in accordance with all requirements of 37 CFR 1.192(c) if the fourth supplemental amendment is entered as indicated.

(5) SUMMARY OF THE INVENTION

The invention discloses a method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process to reduce undercutting of a photoresist layer thereby maintaining design distance between metal lines. (See Field of Invention Specification, paragraph 001; claim 1; Figures 2, items 25 and 26 and Figure 3, items 35 and 36). The method involves the steps of providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof; forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and, depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

(6) ISSUES

1. Is the rejection of claims 1-3, 21, and 23 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al.

(US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

2. Is the rejection of claims 7 and 8 under USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

3. Is the rejection of claim 10 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

4. Is the rejection of claims 11, 13, 19, 22, and 24 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in

view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

5. Is the rejection of claim 15 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

6. Is the rejection of claim 18 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

7. Is the rejection of claim 20 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

(7) GROUPING OF CLAIMS

1. Group I: Claims 1-3, 21, and 23
2. Group II: Claims 7 and 8
3. Group III: Claim 10
4. Group IV: Claims 11, 13, 17, 19, 22, and 24
5. Group V: Claim 15
6. Group VI: Claim 18
7. Group VII: Claim 20

(8) ARGUMENTS

Issue 1

Is the rejection of claims 1-3, 21, and 23 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest

APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

Lin et al. teach a dual damascene process **by filling a via opening** with **protective material** prior to patterning an overlying trench in a dual damascene process (see Abstract). The protective material serves to protect the exposed material at the bottom of the via opening during a subsequent overlying trench etching process (see e.g., col 6, lines 10-14). Lin et al. teach first forming a via opening portion (see e.g., col 4, lines 55-67, col 5, lines 20-25). After removing the via pattern resist layer, Lin et al. teach depositing a protective material disclosed to be a BARC layer e.g., silicon oxynitride or an organic material **to fill the via opening**, (see e.g., col 5, lines 35-57, Figure 2C). Lin et al. then teach **removing a portion** of the protective material **from the filled via opening** to about a level of an intervening etch stop layer following patterning of the overlying trench. The protective material is first etched back followed by etching of the overlying trench or simultaneously etched back with the trench etching (see col 5, lines 57-65 and col 5, lines 1-14).

None of the references citied including Lin et al. disclose or teach APPELLANTS claim 1:

"forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening."

The method of Lin clearly teaches removing an ARC layer from a portion of the via opening prior to patterning a trench opening.

The method of Lin et al. clearly teach filling the via opening with an ARC material **thereby requiring a subsequent etchback process** to remove the ARC filling prior to trench etching to protect the bottom of the via opening (see col 6, lines 7-14).

Examiner argues "**while not specifying an alternative embodiment requiring non-filling of the ARC layer** in the holes or openings, it is readily apparent that adequate protection could

also be obtained by using one or more ARC layers of sufficient thickness without necessarily requiring that the ARC material fill one or more via openings or holes.." . Examiner is impermissibly re-creating APPELLANTS disclosed invention by hindsight reasoning and can point to no suggestion, hint, or desirability in the teachings of Lin et al. of doing what APPELLANTS have accomplished by their claimed invention.

"The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

The teachings of Yu et al. and Filipak et al. do not help Examiner in establishing a *prima facie* case of obviousness with respect APPELLANTS disclosed and claimed invention.

Yu et al. teach a method for etching sub-quarter micron openings in dielectric insulating layers by using a thin layer DUV photoresist (see Abstract). In one embodiment, Yu et al. disclose forming a via opening for filling with a tungsten plug by using a Ti/TiN etching hardmask which also functions as an ARC layer for etching the via opening (col 4, lines 58-62). The via

is then etched with the Ti/TiN layer hard mask providing high selectivity for etching the insulating layer (col 6, lines 19-24).

Yu et al. does not disclose or suggest depositing an ARC layer to fill the via opening as taught by Lin et al., nor disclose or suggest forming an ARC layer formed over sidewalls of a via opening without filling the via opening prior to patterning an overlying trench portion in a dual damascene process as claimed by APPELLANTS. The disclosure of Yu et al. of a Ti/TiN hardmask prior to forming a via opening does not help Examiner in establishing a *prima facie* case of obviousness with respect to APPELLANTS disclosed and claimed invention.

Moreover, there is no apparent reason for combining the teachings of Yu et al. with Lin et al. However, even assuming *arguendo* proper combination of Yu et al. and Lin et al., such combination does not produce APPELLANTS claimed invention.

Filipiak et al. generally discloses types of ARC layers such as silicon oxynitride and titanium nitride in the background of the invention (see col 1, lines 10-20) as well as teaching the use of multiple ARC layers including forming inorganic ARC

layers, e.g., silicon oxynitride with a continuously graded composition or including a plurality of discrete portions to form an antireflective layer (see col 2, lines 17-27, col 3, lines 21-30). There is no apparent motivation for combining Filipiak et al. with either Yu et al. or Lin et al. For example, Filipiak et al. disclose the use ARC layers **prior to** etching via openings, and further, do not disclose a dual damascene process.

Nevertheless, assuming *arguendo*, a proper motivation for combining the references, such combination does not produce APPELLANTS disclosed and claimed invention. Neither Lin et al., Yu et al., nor Filipiak et al. disclose or suggest forming an ARC layer over sidewalls of a via opening without filling the via opening to reduce light reflection in a subsequent overlying trench patterning process as disclosed and claimed by APPELLANTS.

None of the references cited recognizes or solves the problem in a way that APPELLANTS disclosed and claimed invention accomplishes:

"A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process"

Issue 2

Is the rejection of claims 7 and 8 under USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issue 1.

With respect to claim 7, APPELLANTS do not disclose or claim a Ti/TiN layer but rather disclose a TiN ARC layer as one element of a Markush group for forming an ARC layer according to claim 1. Yu et al. do not discuss, disclose or suggest the desirability of depositing an ARC layer to cover the via opening sidewalls without filling the via opening prior to a trench patterning process overlying the via. The disclosure of Yu et al. in forming a Ti/TiN hardmask layer that also functions as an ARC layer does not help Examiner in making out a *prima facie* case of obviousness.

Examiner argues that the prior art disclosed in Lin et al. as shown in Figures 1C through 1F support Examiners argument since "these etch stop materials are also expected to inherently function as ARC layers". Examiner provides no support for this statement of inherency. Lin et al. only disclose the use of SiN as an etch stop layer. Nevertheless, the fact that SiON is well known as having antireflectance properties is irrelevant to the issue of whether APPELLANTS claimed invention has been suggested or disclosed in Lin et al.

"To establish inherency, the extrinsic evidence must make clear that the missing descriptive matter is necessarily present in the thing described in the reference, and that it would be so recognized by persons of ordinary skill." *In re Oelrich, 666 F.2d 578, 581-582, 212 USPQ 323, 326 (CCPA 1981).*

The prior art as disclosed in Lin et al. is referring to a totally different process of manufacturing dual damascenes. The prior art e.g., at col 2, lines 34-52) discloses depositing a **selective etch barrier layer** where SiN or SiON are disclosed to be useful materials with an appropriate etching selectivity. The etch barrier is deposited into **a trench opening** followed by etching **an opening through the etch barrier** at the bottom of the

trench opening **followed by etching the via hole**. The etch barrier disclosed in the prior art by Lin et al. is not suggested or disclosed to have or require an anti-reflective property. However, even assuming arguendo, that such a suggestion was present in Lin et al., the teachings of Lin et al. do not produce APPELLANTS disclosed and claimed invention nor recognize or solve the problem in a way that APPELLANTS have recognized and solved in their claimed invention:

Moreover, the prior art disclosed in Lin et al. that the Examiner relies on, would not work in the method of APPELLANTS since the purpose of the ARC layer in APPELLANTS disclosed and claimed invention is to reduce light reflections in an overlying trench line patterning process **following formation of a via opening**. Indeed, Lin et al. affirmatively teach away from APPELLANTS claimed invention by requiring either a separate or simultaneous etching step to remove a portion of the protective material **during** etching an overlying trench (col 5, line 62 - col 6, line 14). The principal of operation of Lin et al. is completely different than the principal of operation of the method of Lin et al.

"Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art." *In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 1 USPQ2d 1941 (Fed. Cir. 1992).*

"If the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." *In re Ratti, 270 F.2d 810, 123, USPQ 349 (CCPA 1959).*

Issue 3

Is the rejection of claim 10 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issues 1 and 2.

Further, neither Lin et al., Yu et al., nor Filipiak et al. disclose or teach "wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another" in a dual damascene formation process or recognize the problems or suggest a solution for "reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process" with respect to such a structure. The failure of the cited references to recognize the problem with respect to a dual damascene including more than one via opening or suggest a solution to the problem demonstrates the non-obviousness of APPELLANTS disclosed and claimed invention.

APPELLANTS clearly propose the problem in paragraph 006 of the Specification:

"One problem with the dual damascene process, **especially where metal interconnect lines are in a head to head design** thereby making the distance between metal interconnect lines critical as design rules are scaled down, has been the phenomenon of undercutting the photoresist during a photoresist removal process where portions of a photoresist layer have been unintentionally exposed by scattered or reflected light and are removed after photoresist development. **The term "head to head design" is defined as including via openings that are substantially adjacent to one another.**"

Issue 4

Is the rejection of claims 11, 13, 19, and 22 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issues 1-3, above.

Further, none of the cited references suggests or discloses APPELLANTS disclosed and claimed invention including:

"providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer"

prior to forming via openings, or **substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the via openings**, prior to patterning an overlying photoresist layer with trench openings as claimed by APPELLANTS in claim 11.

Further, none of the cited references recognizes or suggests a solution to a problems APPELLANTS have recognized and solved"

"reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process"

None of the cited references or any combination thereof teach, suggest or disclose forming a first ARC layer over the IMD layer **prior** to forming **via openings** followed by **forming** a second ARC layer to cover via opening sidewalls **without filling the via openings** as claimed by APPELLANTS in amended claim 11. Neither do Lin et al. disclose the problem of photoresist undercutting from via sidewall reflections especially in the case where there is more than one via opening.

Examiner argues that "it would also have been obvious to apply at least one thin conformal ARC layer to the sidewalls of the holes or openings without filling the holes or openings before patterning an overlying resist layer to avoid reflective notching of the photoresist, **as taught by Lin and disclosed by Filipiak**".

APPELLANTS assert that Examiner is clearly mistaken that Lin et al. teach such a process or that Filipiak discloses such a

process. Neither Lin et al. nor Filipiak et al. disclose, hint, or suggest **conformally** forming an ARC layer over sidewalls of a via opening without filling the via opening prior to a trench patterning process to reduce light reflection from via sidewalls in the trench patterning process, a problem recognized and solved by APPELLANTS disclosed and claimed invention.

Rather, Lin et al. teach **filling the via opening** with a **protective material** to protect the via bottom portion in a subsequent trench etching process. Yu et al. teach using a Ti/TiN etching hardmask which also functions as an ARC layer **for etching the via opening**. Filipiak et al. teach forming a multiple graded ARC layers over an insulating layer **prior to etching** via openings (see col 5, lines 14-40) and **do not disclose a dual damascene process**. The above teachings individually, or in combination, **do not** make out a *prima facie* case of obviousness nor recognize or solve the problem APPELLANTS have recognized and solved by their disclosed and claimed invention.

The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in

the prior art, and not based on applicant's disclosure." *In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).*

Issue 5

Is the rejection of claim 15 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issues 1, 2 and 4.

Issue 6

Is the rejection of claim 18 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issues 1, 3 and 4.

Issue 7

Is the rejection of claim 20 under 35 USC § 103(a) as being unpatentable over Lin et al. (US 6,042,999) in view of Yu et al. (US 6,027,861) and further in view of Filipiak et al. (US 5,918,147) proper when such references do not teach or suggest APPELLANTS claimed invention or recognize or solve a problem in a way that APPELLANTS have recognized and solved by their claimed invention?

APPELLANTS reiterate the statements made above with respect to Issues 1 and 4.

Further, none of the references cited teach forming a first ARC layer over a first and second dielectric layers prior to forming a via opening, and forming at least one additional ARC layer substantially conformally to cover via opening sidewalls without filling the via opening following formation of a via opening, as claimed by APPELLANTS, in claim 20 (second dielectric layer).

None of the cited references or any combination thereof suggest or discloses the problem that APPELLANTS have recognized nor suggest or disclose a solution that solves the recognized problem in the way that APPELLANTS have solved it by their disclosed and claimed invention, thereby demonstrating the non-obviousness of APPELLANTS disclosed and claimed invention.

CONCLUSION

Examiner has not met his burden of establishing a *prima facie* case of obviousness and moreover, APPELLANTS disclosed and claimed invention has been demonstrated to be nonobvious. None of the cited references individually or in combination recognizes and solves the problem of light reflections from via opening sidewalls to undercut a resist layer in a trench patterning process, by covering via opening sidewalls with an ARC without filling the via openings. The fact that Examiner can produce no references disclosing or suggesting APPELLANTS disclosed and claimed invention strongly supports a conclusion of nonobviousness.

"We do not pick and choose among the individual elements of assorted prior art references to recreate the claimed invention,

but rather we look for some teaching or suggestion in the references to support their use in a particular claimed combination" *Symbol Technologies, Inc. v. Opticon, Inc., 935 F.2d 1569, 19 USPQ2d 1241 (Fed. Cir. 1991).*

It is therefore respectfully submitted that Examiners final rejection of Appellants claims is improper under the statutory standard of 35 USC § 103(a) as interpreted by both the Board and the Courts.

The reversal of the final rejection is respectfully solicited from the Board.

Respectfully submitted,

Tung & Associates

Randy W. Tung (31,311)

CLAIM APPENDIX

1. A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof;

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

2. The method according to claim 1, wherein an etching stop layer is provided over said IMD layer.

3. The method of claim 2, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

4. - 6. (cancelled)

7. The method of claim 1, wherein the ARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

8. The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. (cancelled)

10. The method of claim 1, wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. A method of reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming via openings extending through a thickness portion of the IMD layer;

substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the one via openings; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over one or more of the via openings.

12. (cancelled)

13. The method of claim 11, wherein an etching stop layer is provided over the IMD layer underlying the first ARC layer.

14. The method of claim 13, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

15. The method of claim 11, wherein the first and second ARC layers are selected from the group consisting of silicon oxynitride and titanium nitride.

16. (cancelled)

17. The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. The method of claim 11, wherein said via openings are formed substantially adjacent to one another.

19. The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process comprising the steps of:

forming a first dielectric layer over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

photolithographically patterning a trench opening over the at least one via opening.

21. The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

24. The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. - 26. (cancelled)

U.S.S.N. 09/941,537

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants: Chen et al. Group Art Unit: 1756

Serial No.: 09/941,537 Examiner: J. S. Ruggles

Filed: 08/29/2001 In Response to Office Action Dated: 06/25/2004

For: METHOD FOR REDUCING LIGHT REFLECTANCE IN A PHOTOLITHOGRAPHIC DUAL DAMASCENE TRENCH PATTERNING PROCESS

Attorney Docket No.: 67,200-477

EXPRESS MAIL CERTIFICATE

"Express Mail" label number EV 525 156 546 US
Date of Deposit July 21, 2004

I hereby certify that this paper in triplicate and a credit card payment form in the amount of $330.00 (required filing fee) are being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR §1.10 on the date indicated above and is addressed to: Mail Stop: Appeal, Commissioner for Patents, Alexandria, VA 22313-1450

Kathy Dixon

FOURTH SUPPLEMENTAL AMENDMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, Va 22313-1450

Dear Sir:

In response to Advisory Actions mailed 04/06/2004 and 6/25/2004 Applicants respectfully request entry of the following amendments to remove issues from Appeal and comply with Examiners requirements and/or suggestions. Please consider the following remarks.

Abstract Amendments

Please replace the Abstract at paragraph 0045 beginning at page 25 with the following replacement paragraph submitted on a separate sheet as follows:

0045 A method for reducing light reflectance in a photolithographic dual damascene trench patterning process [[is]] ~~disclosed~~ including providing an inter-metal dielectric (IMD) layer including at least one via opening extending through a thickness thereof; and, conformally forming an antireflectance coating (ARC) layer over ~~said~~ the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening to reduce light reflectance.

Specification Amendments

Please replace paragraphs 007 beginning at page 4 with the following rewritten paragraph:

007 Typically, in a dual damascene manufacturing process known in the art as a via-first-trench last process conventional photolithographic processes using a photoresist layer [[is]] are first used to pattern and expose an etching mask which is used for etching via openings through the IMD layer. Subsequently a similar process is used to define trench openings that are formed substantially over the via openings which in turn define metallic interconnect lines. [[t]]The via openings and trench openings are subsequently filled with metal to form metalization vias and metal interconnect lines. The surface may then be planarized by conventional techniques to better define the metal interconnect lines and prepare the substrate for further processing.

Please replace the paragraph 0042 beginning on page 18 with the following rewritten paragraph:

0042 The photoresist layer [[36]] 37 serving to define the trench opening pattern [[38]] 39 is preferably from ~~5000 to 9000~~ 1000 to 20000 Angstroms. It will further be appreciated by those skilled in the art that positive photoresist is the preferable photoresist.

Please replace paragraph 008 on page 4 with the following rewritten paragraph:

0008 During the photolithography process, undercutting the photoresist layer acts to decrease the spacing between metallic lines[[,]] and compromises device design. As an example of compromised electrical property functionality, the distance between metal interconnect lines may be decreased such that leakage current by a tunneling mechanism may occur. Further, undercutting the photoresist layer acts to weaken the mechanical integrity of the remaining photoresist lines, thereby increasing the possibility of photoresist line failure. In addition, even if the photoresist line doesn't fail, a dielectric insulating material made thinner as a result of undercutting may be structurally weakened and may lead to insulation failure in a resulting semiconductor device. In any case, the integrity of

subsequent steps in the dual damascene process is [[are]] compromised.

Please replace paragraph 0010 on page 4 with the following rewritten paragraph:

0010 Typically, an antireflectance coating (ARC) layer 15 may be formed over the etching stop layer 14 prior to the conventional photolithographic process used for patterning the via openings 12a, 12b. The ARC layer 15 reduces the effect of light reflection undesirably exposing a photoresist overlayer 16 used for defining via openings 12a, 12b. Light reflection (scattering) from, for example, the IMD layer 10 surface, etching stop layer 14 surface, and their respective interfaces, can cause undesired light exposure of an overlying photoresist layer 16 in a photolithographic masking and patterning steps, for example, in the formation of via openings 12a, 12b. As a result, upon development and removal of the exposed photoresist the phenomenon of undercutting (removing photoresist exposed by reflected light in the foot area of the photoresist) will detrimentally affect the design integrity of the manufactured device.

Please replace paragraph 0015 on page 9 with the following rewritten paragraph:

0015 One solution to the problem of undercutting would be to increase the distance between the trench line patterns or decrease the metal line thickness thereby lessening any mechanical weakening effect due to undercutting. Neither of these proposed solutions, however, is [[are]] compatible with the trend and necessity of continually scaling down structure size. Another solution would be to apply an ARC layer in such a way to avoid the effect of undesired light scattering and reflections from via edges and sidewalls.

Listing of the Claims

Please amend claims 11 and 15 as follows.

Please cancel claims 25 and 26 as follows.

1. (previously presented) A method for reducing light reflectance from via sidewalls in a photolithographic trench patterning dual damascene process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising at least one via opening extending through a thickness thereof;

forming an antireflectance coating (ARC) layer over the IMD layer such that the ARC layer is formed over sidewalls of the at least one via opening without filling the at least one via opening; and,

depositing a photoresist layer over the IMD layer and photolithographically patterning a trench opening over the at least one via opening.

2. (previously presented) The method according to claim 1, wherein an etching stop layer is provided over said IMD layer.

3. (previously presented) The method of claim 2, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

4. - 6. (cancelled)

7. (previously presented) The method of claim 1, wherein the ARC layer is selected from the group consisting of silicon oxynitride and titanium nitride.

8. (previously presented) The method of claim 1, wherein the ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

9. (cancelled)

10. (previously presented) The method of claim 1, wherein the at least one via opening includes at least two via openings formed substantially adjacent to one another.

11. (currently amended) A method of reducing photoresist undercutting due to via sidewall light reflections in a dual damascene trench patterning process comprising the steps of:

providing an inter-metal dielectric (IMD) layer comprising a first anti-reflectance coating (ARC) layer over the IMD layer;

forming via openings extending through a thickness portion of the IMD layer;

substantially conformally depositing a second ARC layer over said IMD layer and the via openings to cover the via opening sidewalls without filling the [[one]] via openings; and,

forming a photoresist layer over the IMD layer and photolithographically patterning trench openings disposed at least partially over ~~one or more of~~ the via openings.

12. (cancelled)

13. (previously presented) The method of claim 11, wherein an etching stop layer is provided over the IMD layer underlying the first ARC layer.

14. (previously presented) The method of claim 13, wherein the etching stop layer is selected from the group consisting of silicon oxynitride and silicon nitride.

15. (currently amended) The method of claim 11, wherein the ~~first and~~ second ARC layer[[s]] [[are]] is selected from the group consisting of silicon oxynitride and titanium nitride.

16. (cancelled)

17. (previously presented) The method of claim 11, wherein the second ARC layer is formed within a range of thickness from about 100 Angstroms to about 1000 Angstroms.

18. (previously presented) The method of claim 11, wherein said via openings are formed substantially adjacent to one another.

19. (previously presented) The method of claim 11, further comprising repeating said method as part of a manufacturing process to form a multi-level interconnected semiconductor structure.

20. (previously presented) An improved method of reducing light reflectance from via sidewalls in a dual damascene trench patterning process comprising the steps of:

forming a first dielectric layer over an underlying substrate;

forming at least one second dielectric layer over said first dielectric layer;

forming at least one anti-reflectance coating (ARC) layer over the at least one dielectric layer;

forming at least one via opening through a thickness of the ARC layer, the at least one second dielectric layer, and the first dielectric layer;

forming at least one additional ARC layer substantially conformally over the at least one ARC layer and the at least one via opening to cover the at least one via opening without filling the at least one via opening;

forming a layer of photoresist over the at least one additional ARC layer; and,

photolithographically patterning a trench opening over the at least one via opening.

21. (previously presented) The method of claim 1, wherein the ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

22. (previously presented) The method of claim 11, wherein at least the second ARC layer is deposited according to a plasma enhanced chemical vapor deposition (PECVD) process.

23. (previously presented) The method of claim 1, wherein the ARC layer consists essentially of silicon oxynitride.

24. (previously presented) The method of claim 11, wherein the first and second ARC layers consist essentially of silicon oxynitride.

25. - 26. (cancelled)

Remarks

Applicants respectfully request entry of the following amendments as previously suggested by Examiner in Final Rejection of 9/11/2003 to remove issues from Appeal as Examiners Advisory Action in Response to Applicants previously submitted first, second, and third Supplemental Amendments after Final Rejection indicate the amendments have not been entered due in part to an inadvertent typographical errors including in claim 11 wherein the last paragraph was repeated and in failing to use double bracketing for deletions.

Applicants have corrected grammatical errors in claim 11, as suggested by Examiner in Final Rejection of 9/11/2003, to overcome Examiners Rejection under 35 USC 112, second paragraph, as well as cancelled claims 25 and 26 to overcome Examiners Objections and Rejections. Applicants have amended claim 15 in accordance with Examiners requirement in Final Rejection of 9/11/2003, thereby removing the issue of Rejection of claim 15 under 35 USC 112, second paragraph.

Applicants have also submitted amendments to the Specification as suggested by Examiner in Final Rejection of 9/11/2003 and as submitted in Applicants first, second, and third

supplemental amendments in addition to adding double brackets for deletions in the instant amendment.

More specifically, the Abstract has been amended and a replacement paragraph presented on a separate page as required under revised amendment practice according to 37 CFR 1.121 as suggested by Examiner.

Claim 11 has been amended to correct grammatical errors thereby removing the basis of Examiners objection and rejection under section 112, second paragraph, by changing the reference to "one via openings" to "the via openings" and changing the reference to "one or more via openings" to "the via openings" making these portions consistent with antecedent portions of the claim and dependent claims. Claims 25 and 26 have been cancelled to overcome Examiners Objection that these claims fail to further limit claims 1 and 11.

Claim 15 has been amended in accordance with Examiners requirement to overcome rejection under 35 USC Section 112, second paragraph.

In response to the most recent Advisory Action of 6/25/04, and Notice of Non-Compliance, Applicants have now listed claims

25 and 26 as cancelled in the Claims Appendix of the Appeals Brief consistent with the instant amendment. Examiner has indicated in the Notification of Non-Compliance mailed 6/25/04, and in a telephone conversation on 7/1/004, that the instant amendment will be entered assuming that the **only additional** changes made in the instant amendment are the addition of **double brackets** for deletion amendments as required by Examiner. Applicants have made **only** these **additional** changes in the instant amendment as required by Examiner and assume the instant amendment will be entered as indicated by Examiner.

In the event that there is some other issue that can be resolved prior to Appeal, or for any other reason, the Examiner is respectfully invited to call the Applicants' representative at his Bloomfield Hills, Michigan office at (248) 540-4040 such that necessary action may be taken to place the application in a condition for Appeal.

Respectfully submitted,

Tung & Associates

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